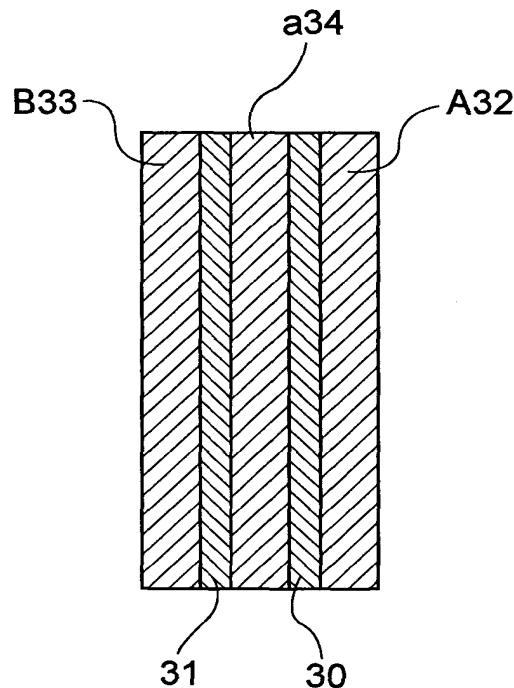
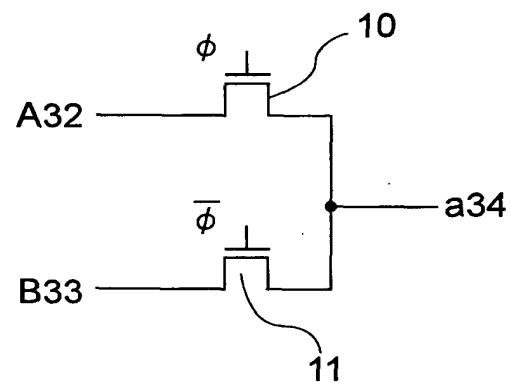


FIG. 1



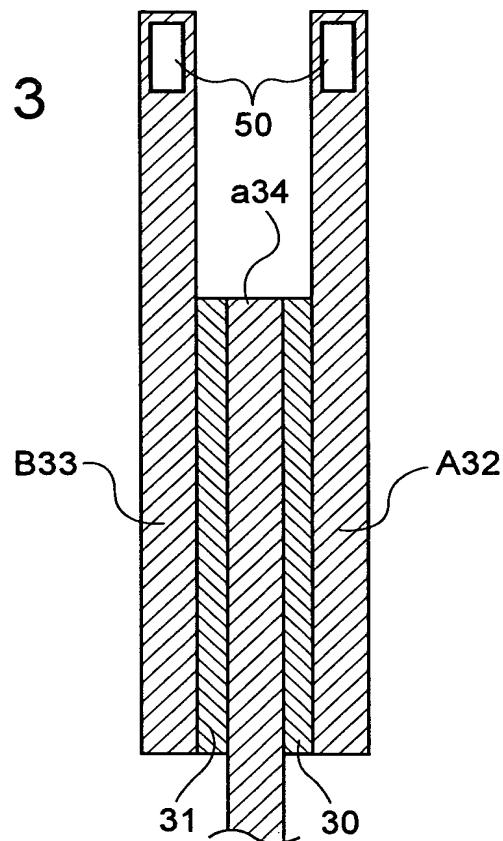
LAYOUT ACCORDING TO FIRST
ENBODIMENT

FIG. 2



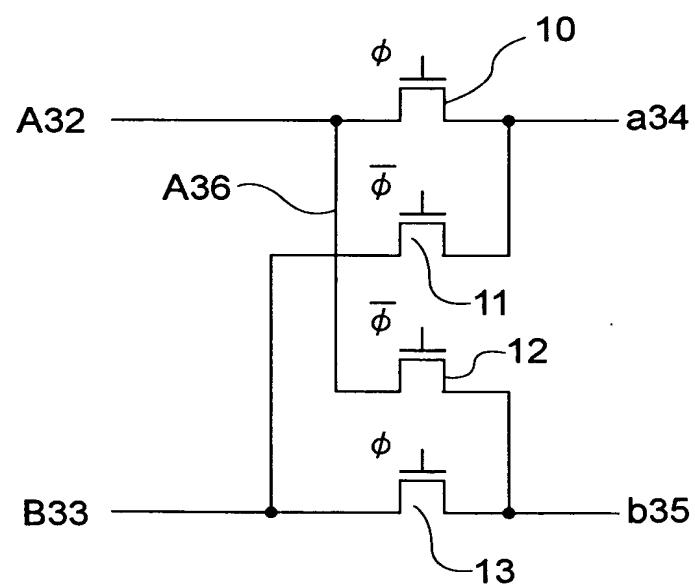
WIRING SWITCH CIRCUIT

FIG. 3



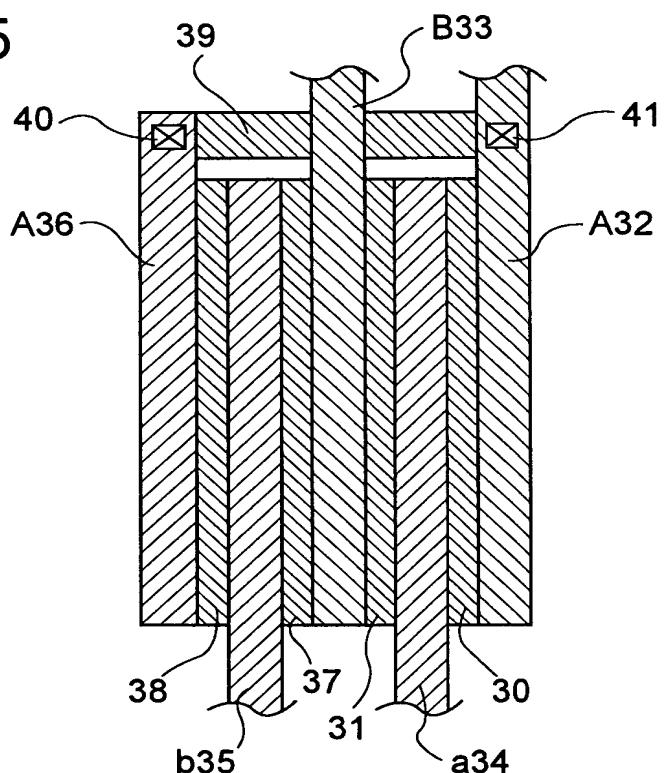
LAYOUT ACCORDING TO SECOND
ENBODIMENT

FIG. 4



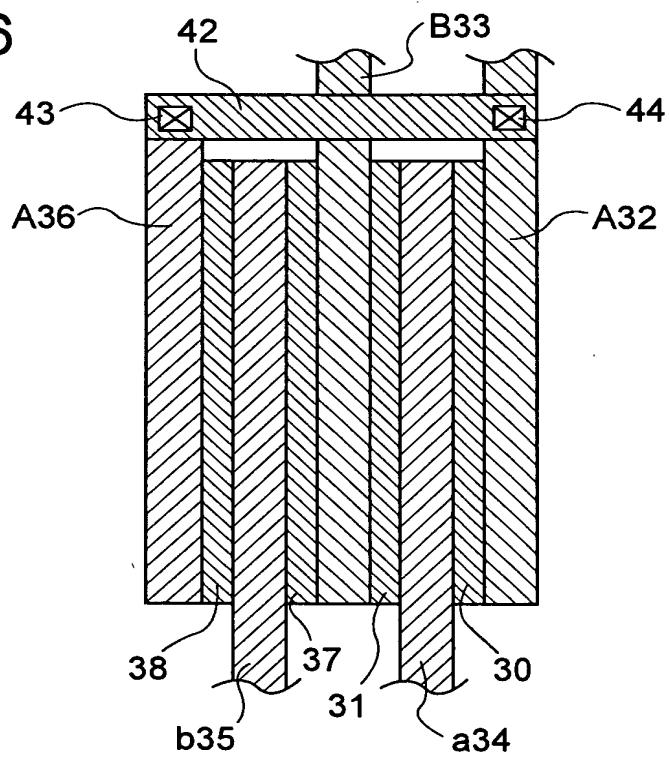
WIRING SWITCH CIRCUIT

FIG. 5



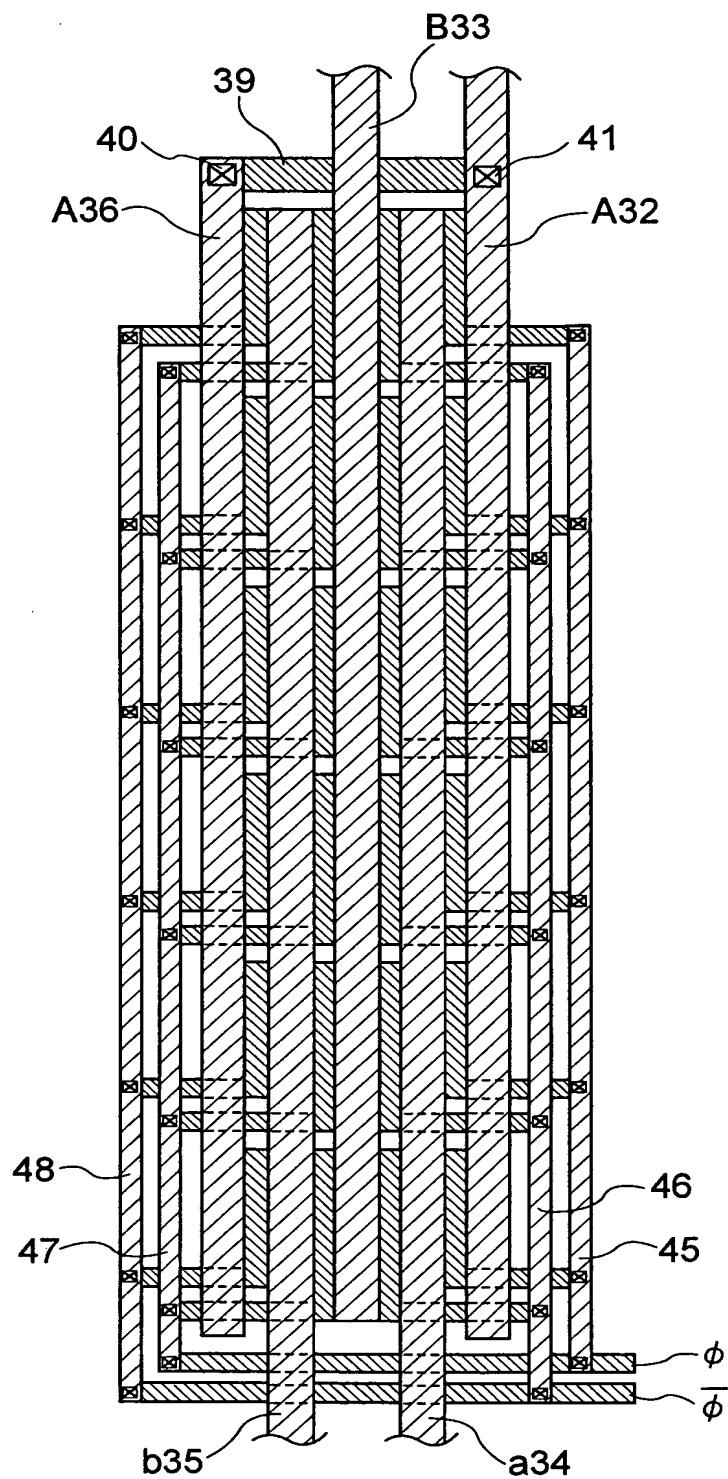
LAYOUT ACCORDION TO THIRD
ENBODYMENT

FIG. 6



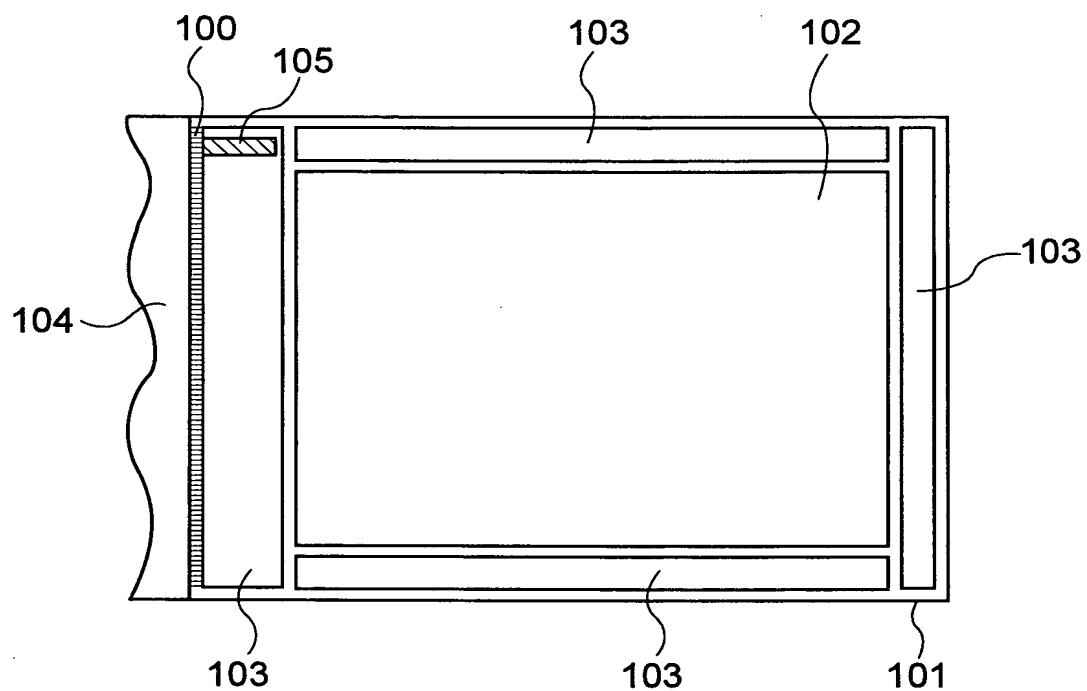
LAYOUT ACCORDION TO THIRD
ENBODYMENT

FIG. 7



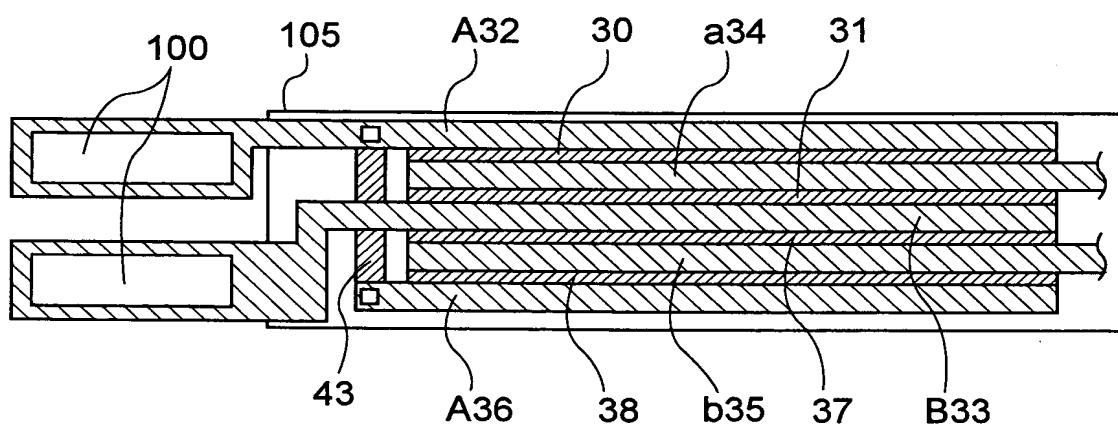
LAYOUT ACCORDING TO FOURTH
ENBODYMENT

FIG. 8



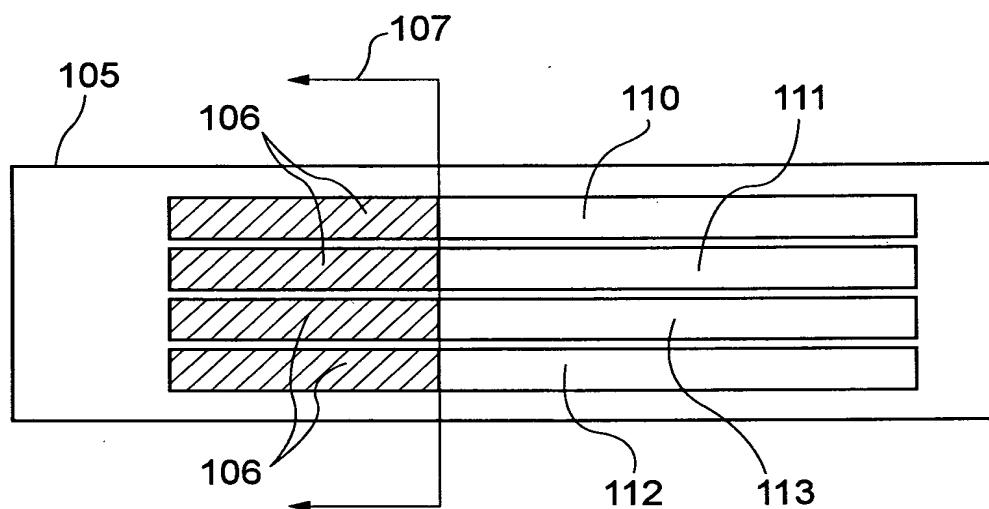
EXAMPLE OF CIRCUIT LAYOUT OF DISPLAY OR
SENSOR ACCORDING TO FIFTH EMBODIMENT

FIG. 9



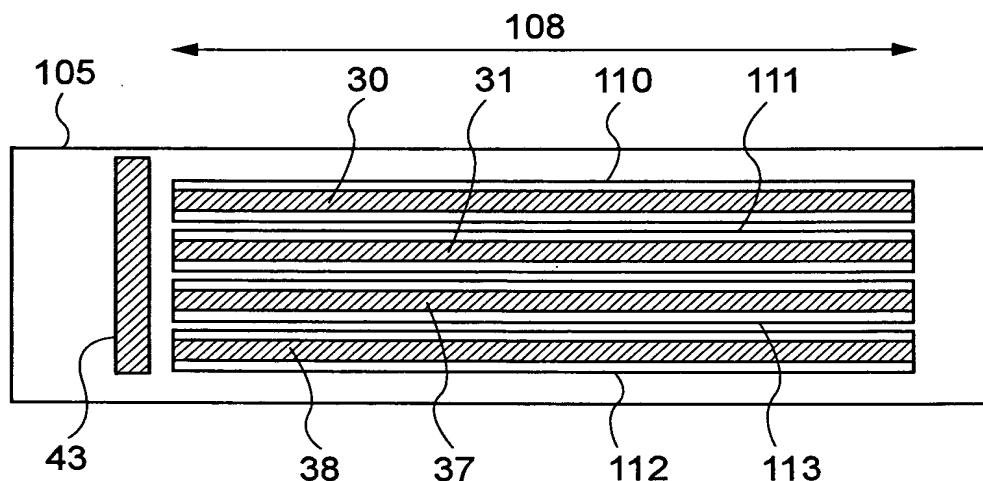
ENLARGED DIAGRAM OF CIRCUIT LAYOUT OF
DISPLAY OR SENSOR

FIG. 10



SILICON POLYCRYSTALLIZATION FOR THIN - FILM
TRANSISTOR CIRCUIT

FIG. 11



GATE ELECTRODE FORMING STEP FOR
THIN - FILM TRANSISTOR CIRCUIT

FIG. 12

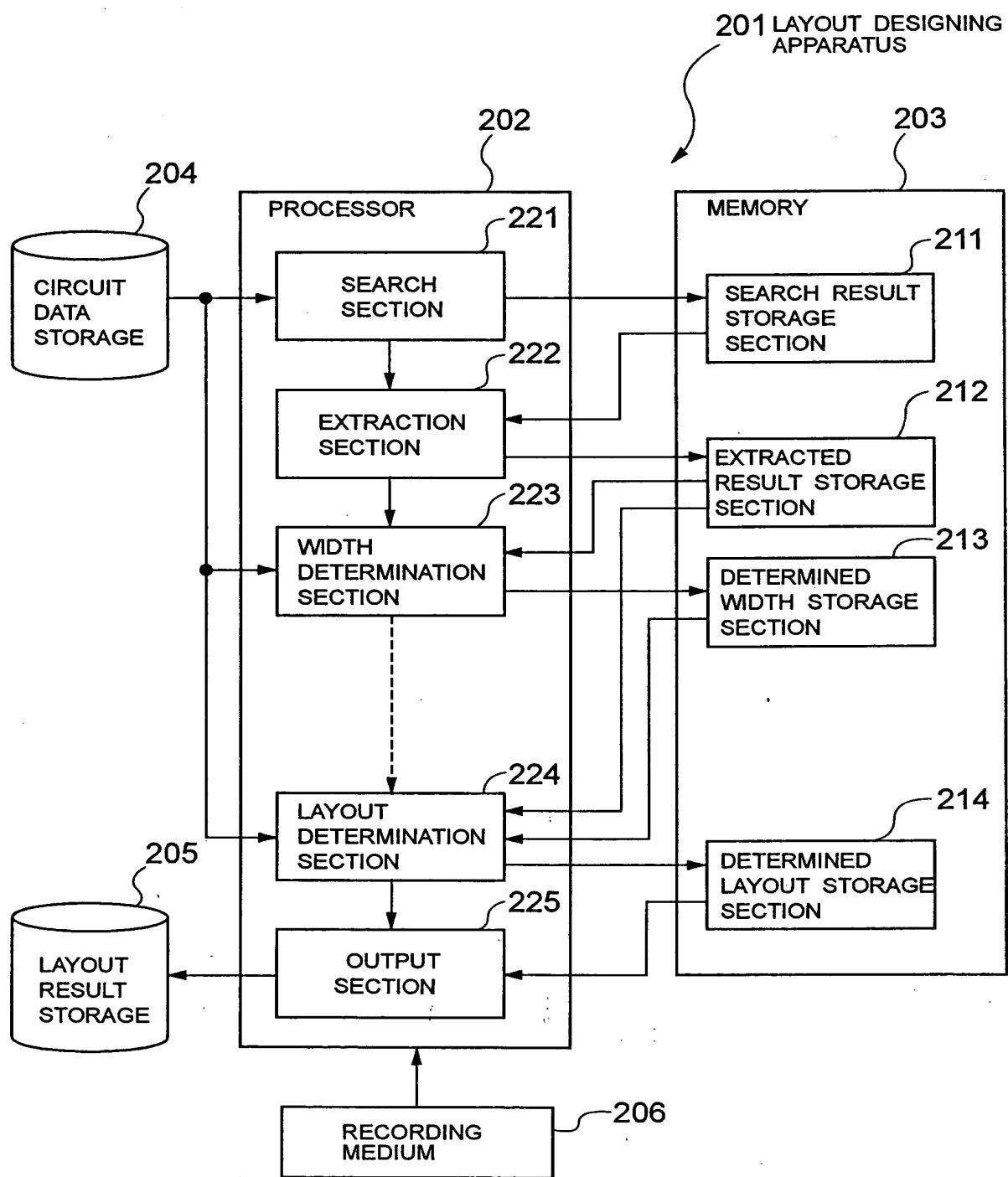


FIG. 13

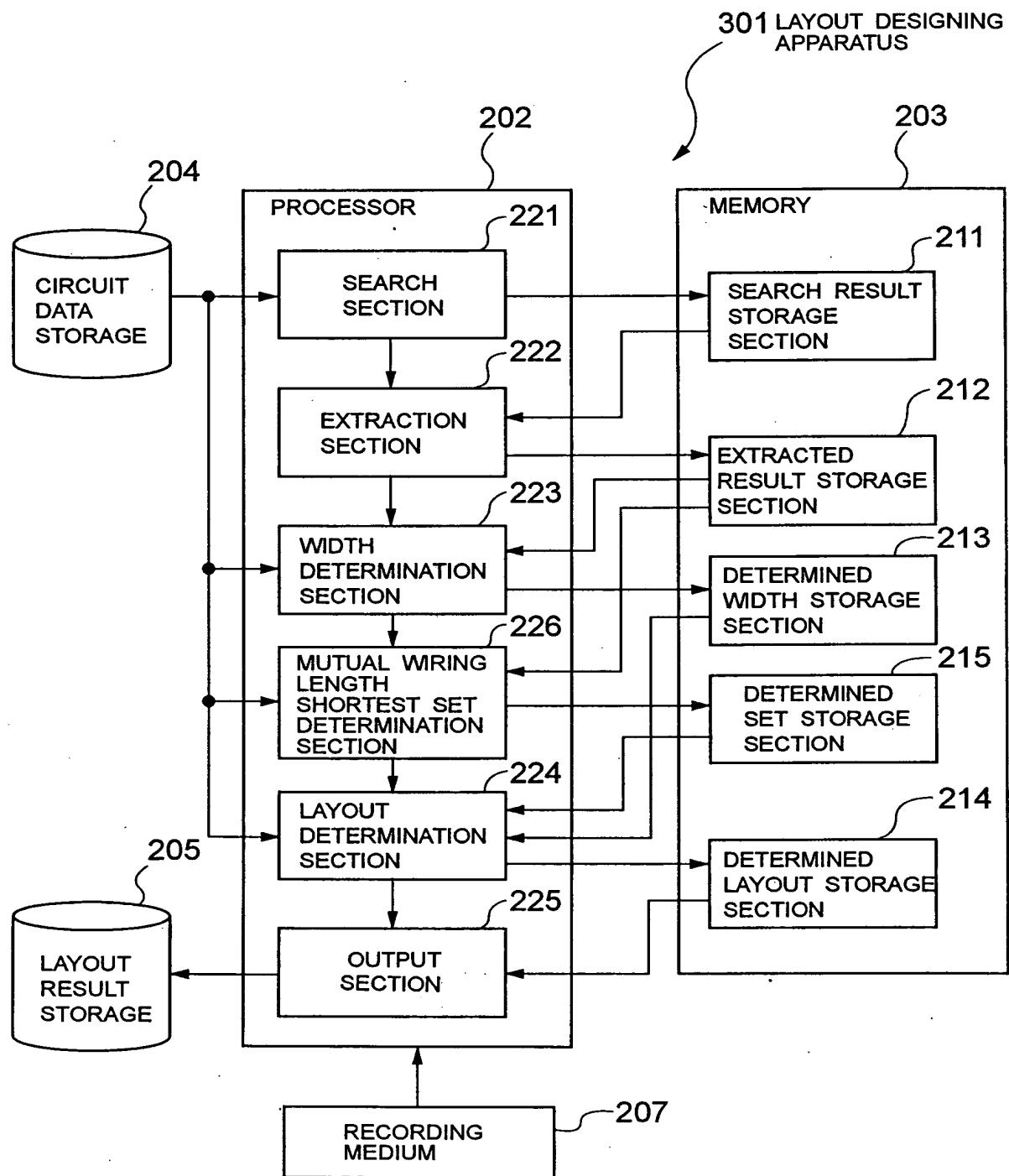


FIG. 14

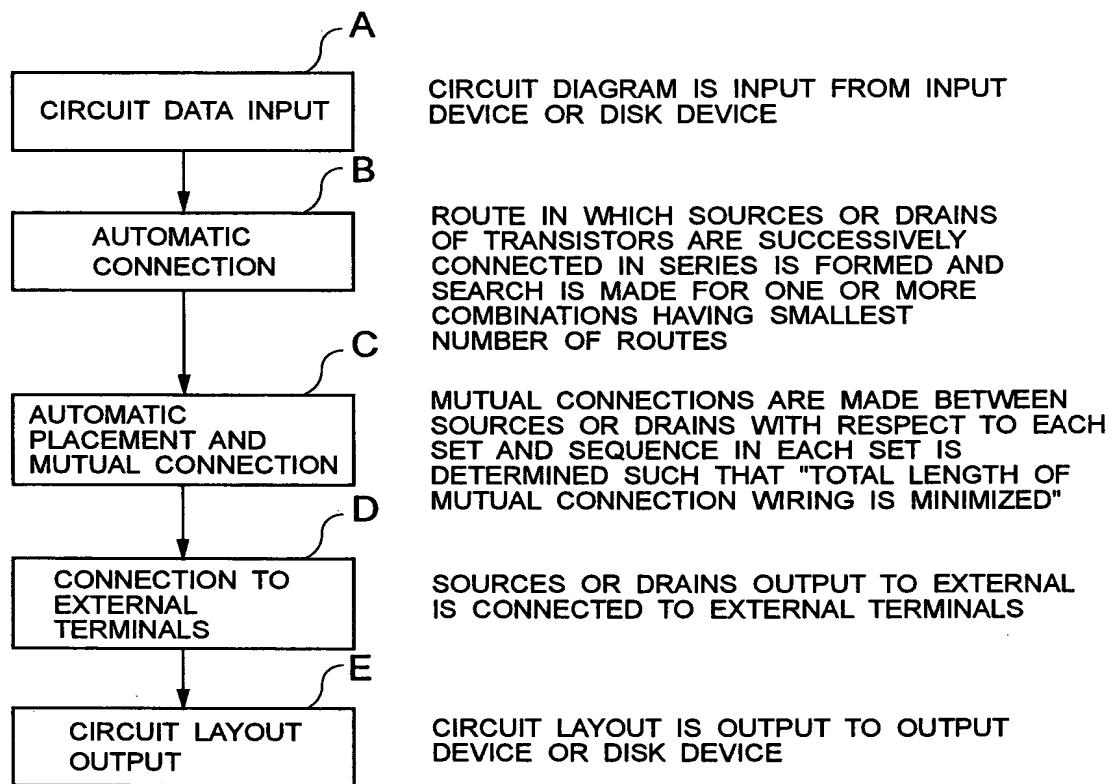
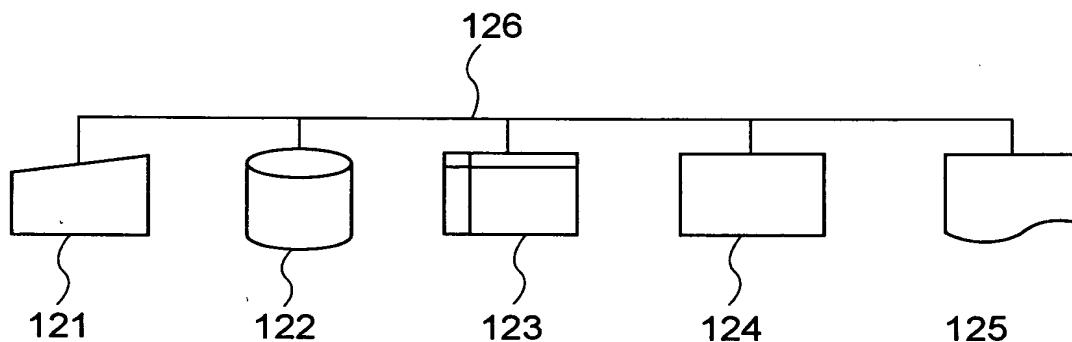
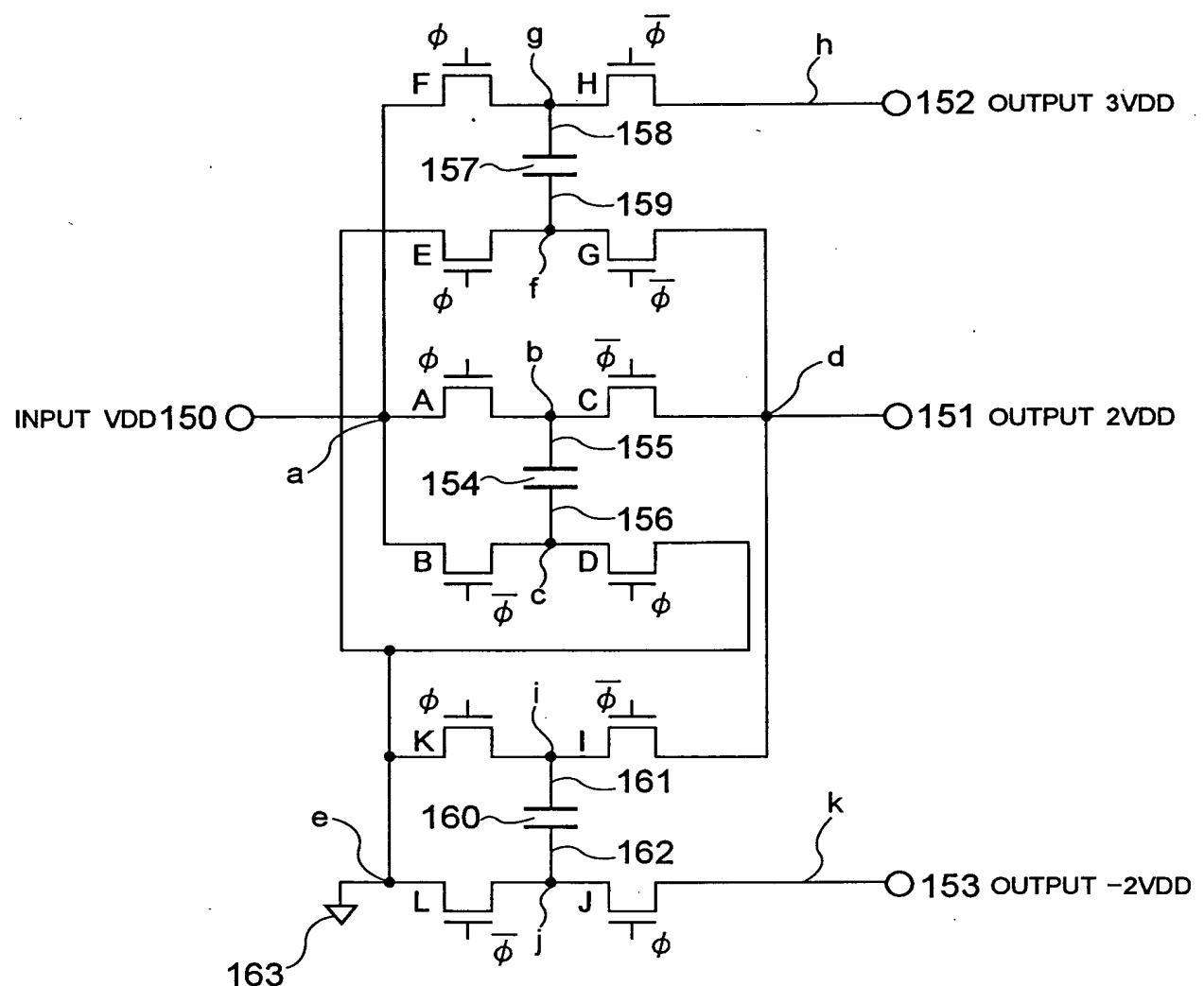


FIG. 15



SYSTEM BLOCK DIAGRAM OF AUTOMATIC LAYOUT FORMATION

FIG. 16



CHARGE-PUMP-TYPE VOLTAGE BOOSTING CIRCUIT

FIG. 17

CONNECTED NODES		CONNECTED NODE ARRAY N				CONNECTED TREE ARRAY T			
		1	2	3	4	1	2	3	4
a	A	B	C	D	F	a	b	c	g
b	A	C				b	a	d	
c	B		D			c	a	e	
d	C		G	I	L	d	b	f	i
e	D		E	K	L	e	c	f	j
f		G	E			f	d	e	
g	F			H		g	a	h	
h				H		h	g		
i			I	K		i	d	e	
j				L		j	e	k	
k					J	k	j		
OBJECT NODES									

CONNECTED TREE (TRANSISTOR)

TWO - DIMENSIONAL CIRCUIT NETWORK MAP, CONNECTED NODE ARRAY, AND CONNECTED TREE ARRAY

FIG. 18

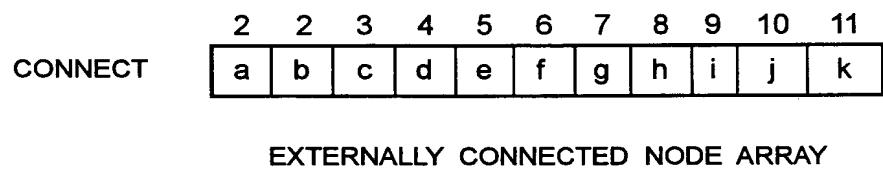
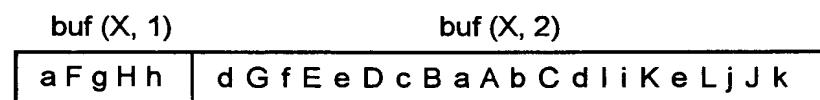
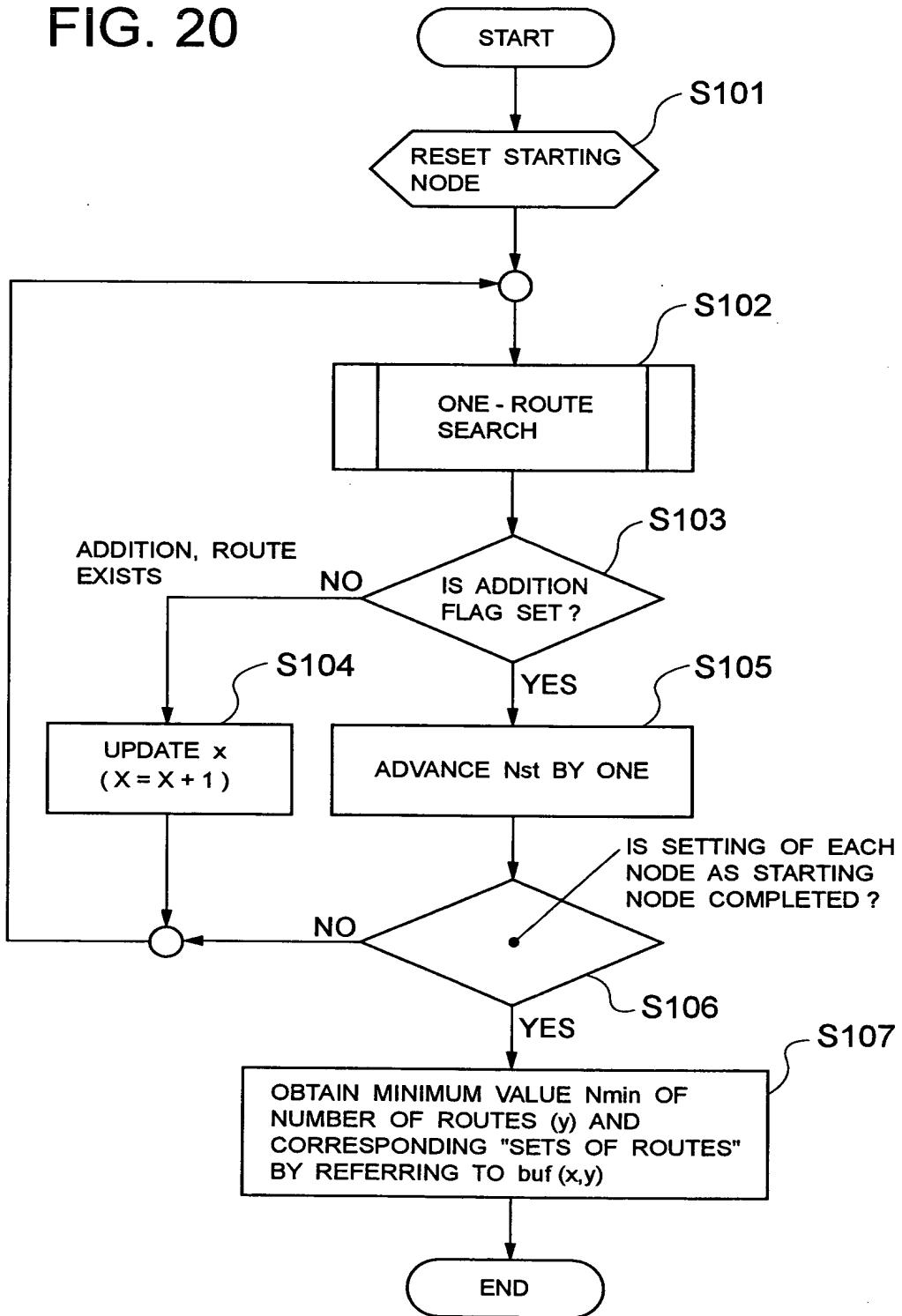


FIG. 19



EXAMPLE OF DATA ON "SET OF ROUTES"

FIG. 20



AUTOMATIC CONNECTION
(ALL NODE SEARCH FLOWCHART)

FIG. 21
ONE-ROUTE (WRITTEN WITH SINGLE STROKE)
SEARCH FLOWCHART

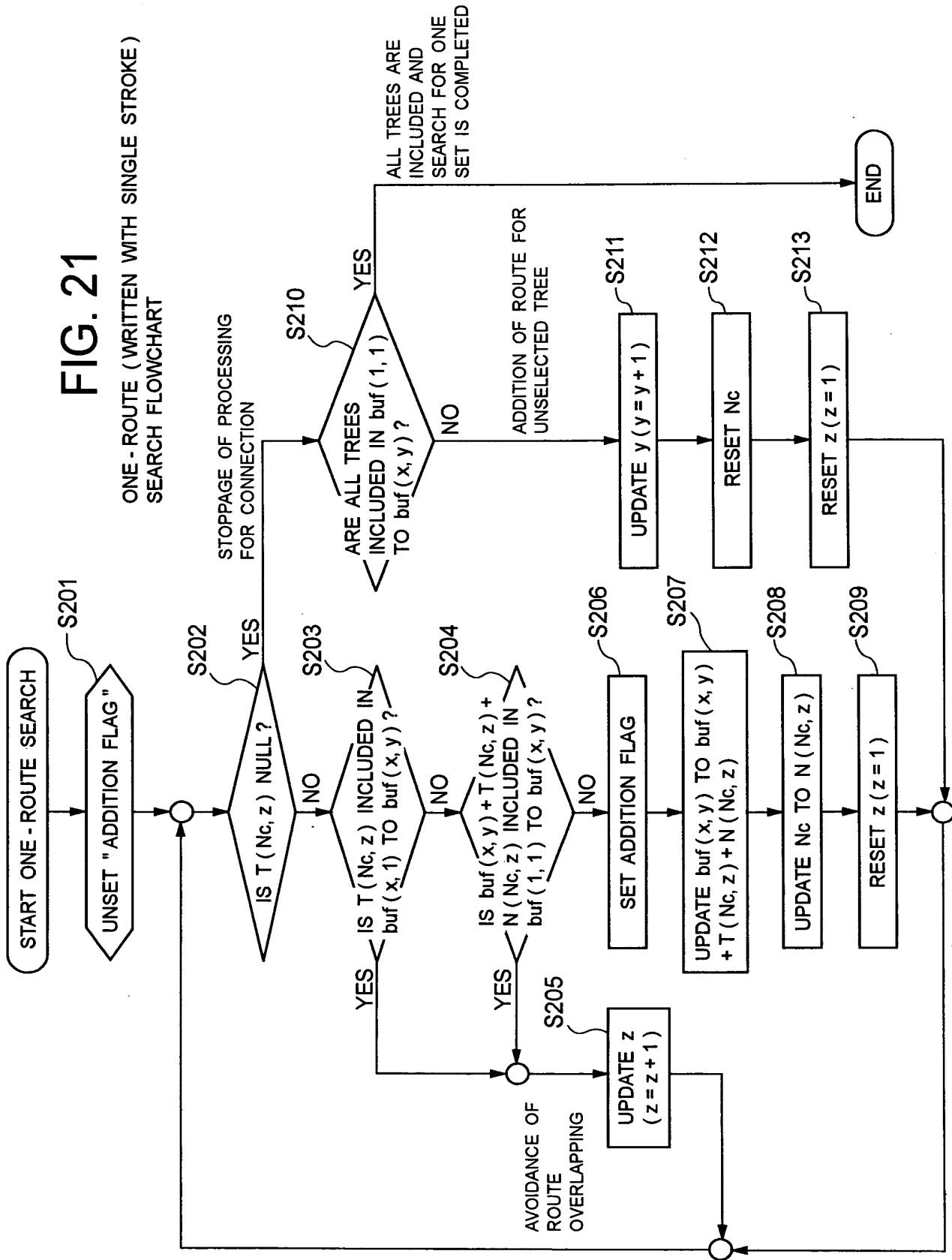


FIG. 22

Nmin = 2

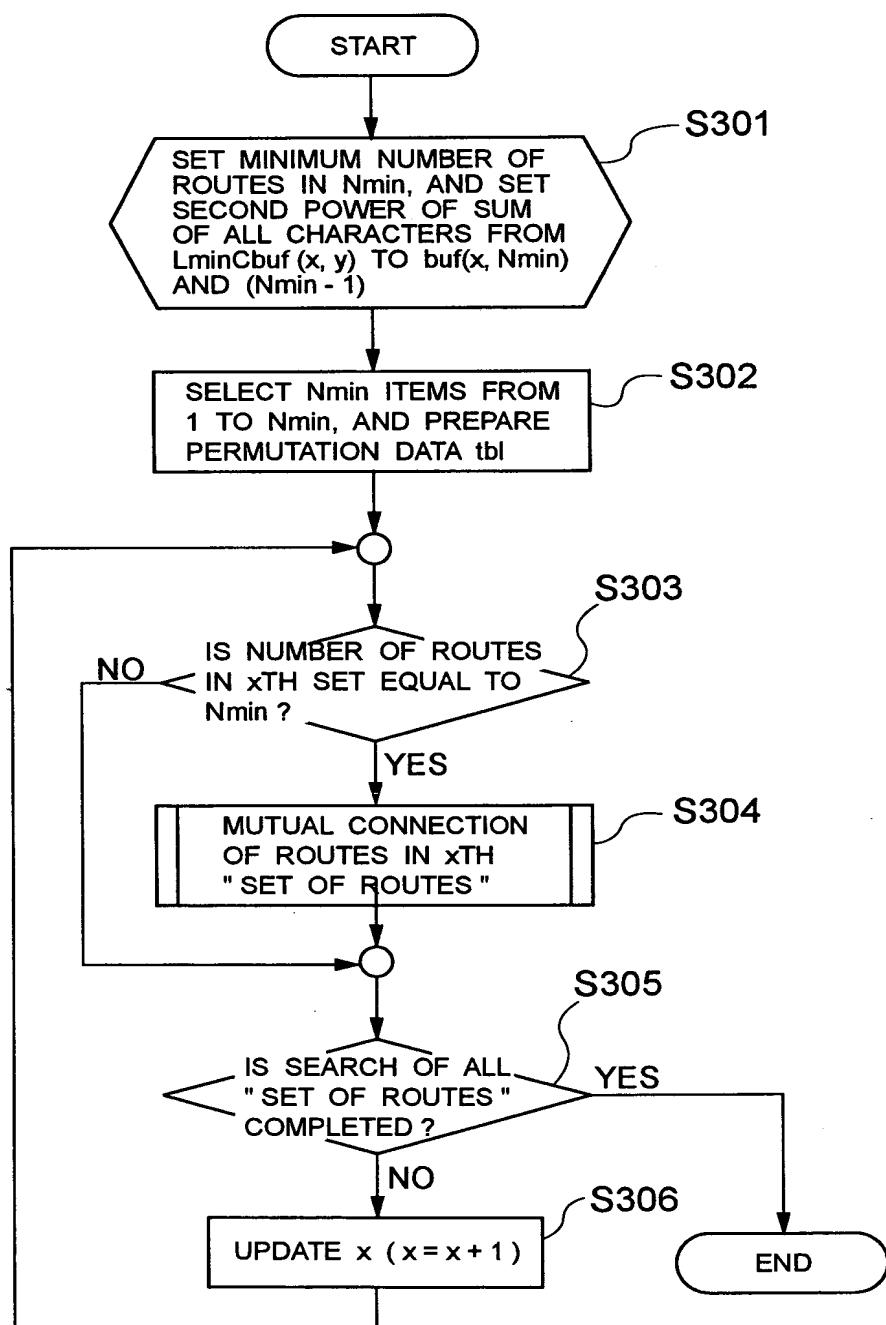
tbl	1	2
1	1	2
2	2	1

Nmin = 3

tbl	1	2	3
1	1	2	3
2	1	3	2
3	2	1	3
4	2	3	1
5	3	1	2
6	3	2	1

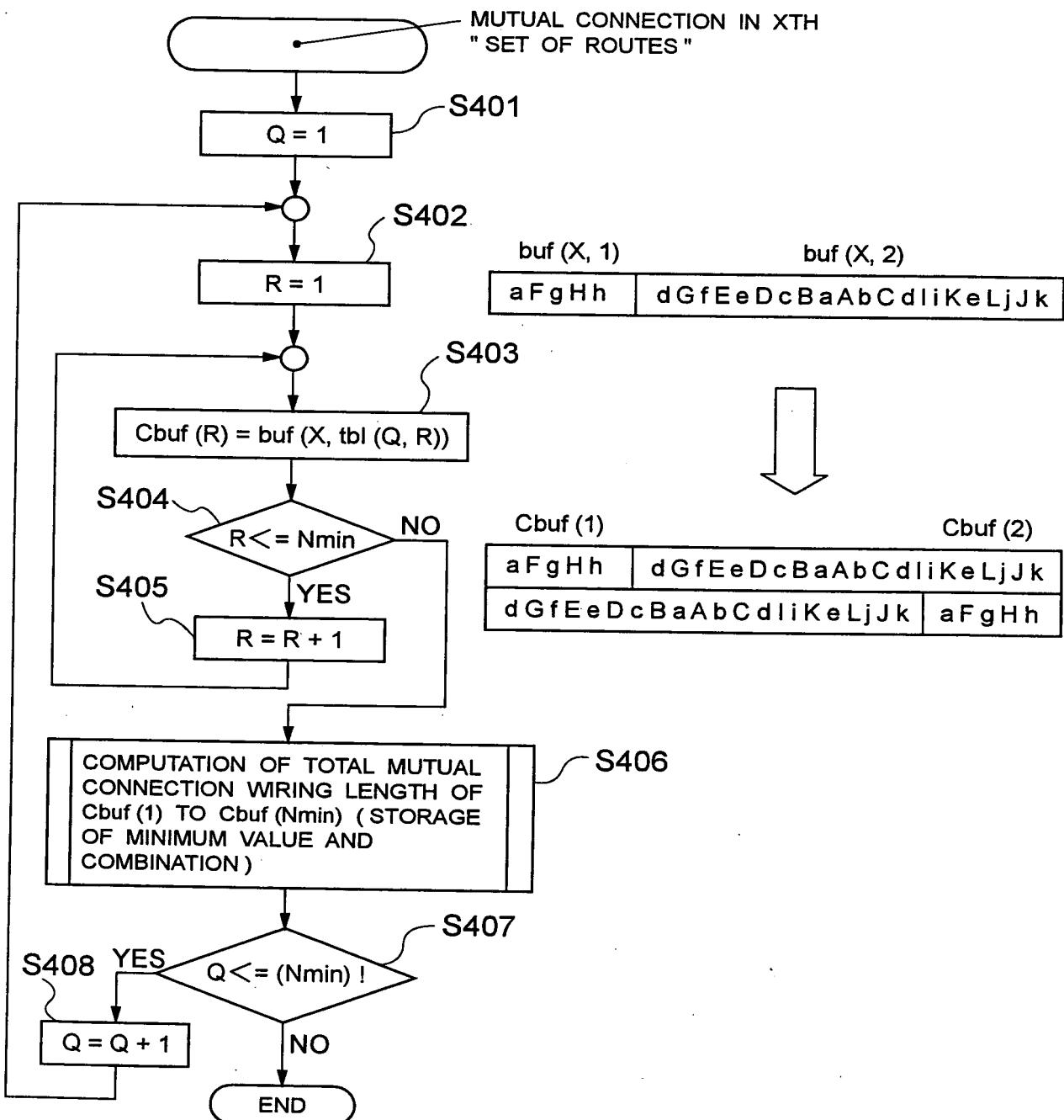
EXAMPLE OF PERMUTATION DATA tbl

FIG. 23



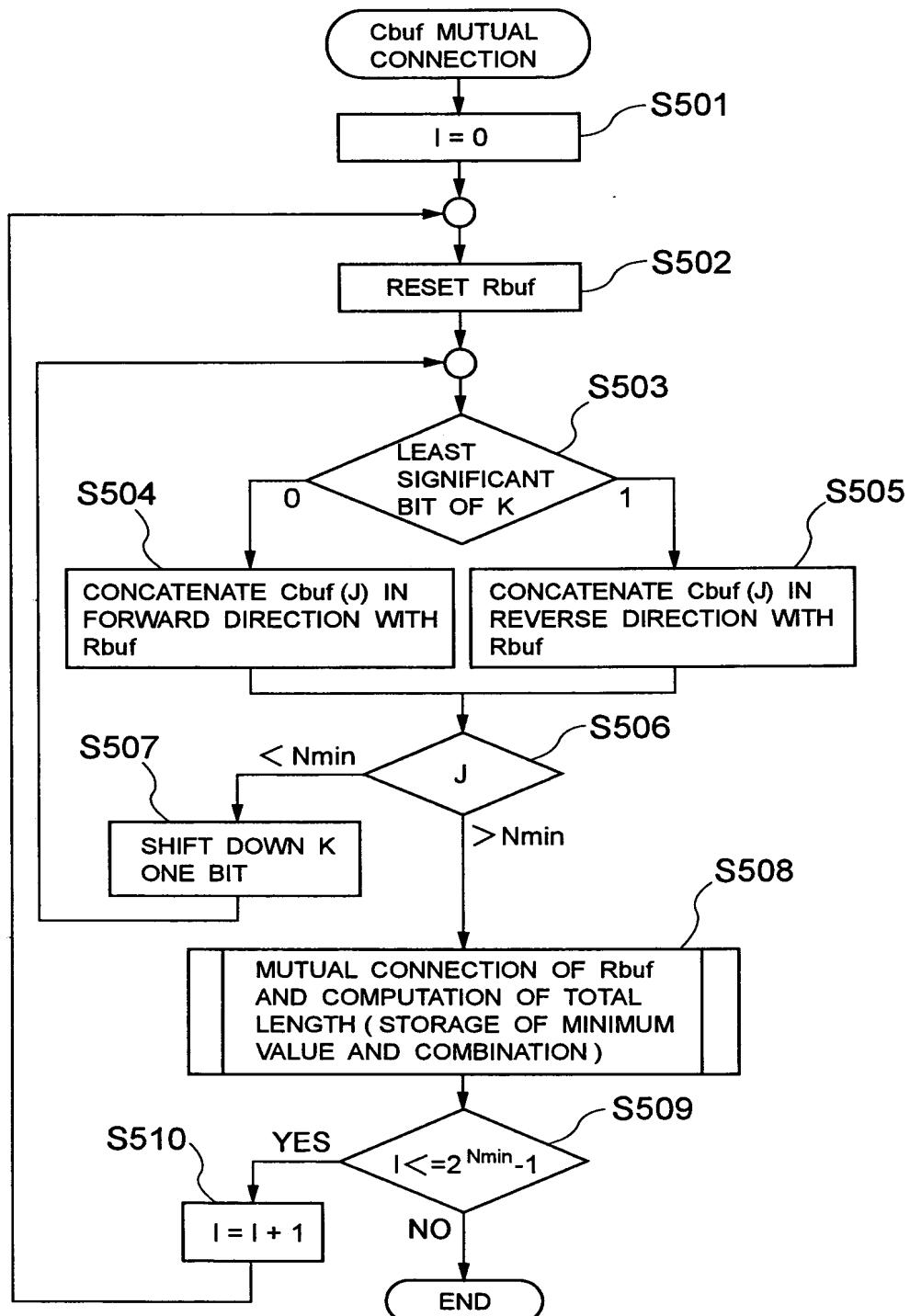
FLOWCHART OF MUTUAL CONNECTION

FIG. 24



FLOWCHART OF MUTUAL CONNECTION IN XTH SET OF ROUTES

FIG. 25



FLOWCHART OF Cbuf MUTUAL CONNECTION

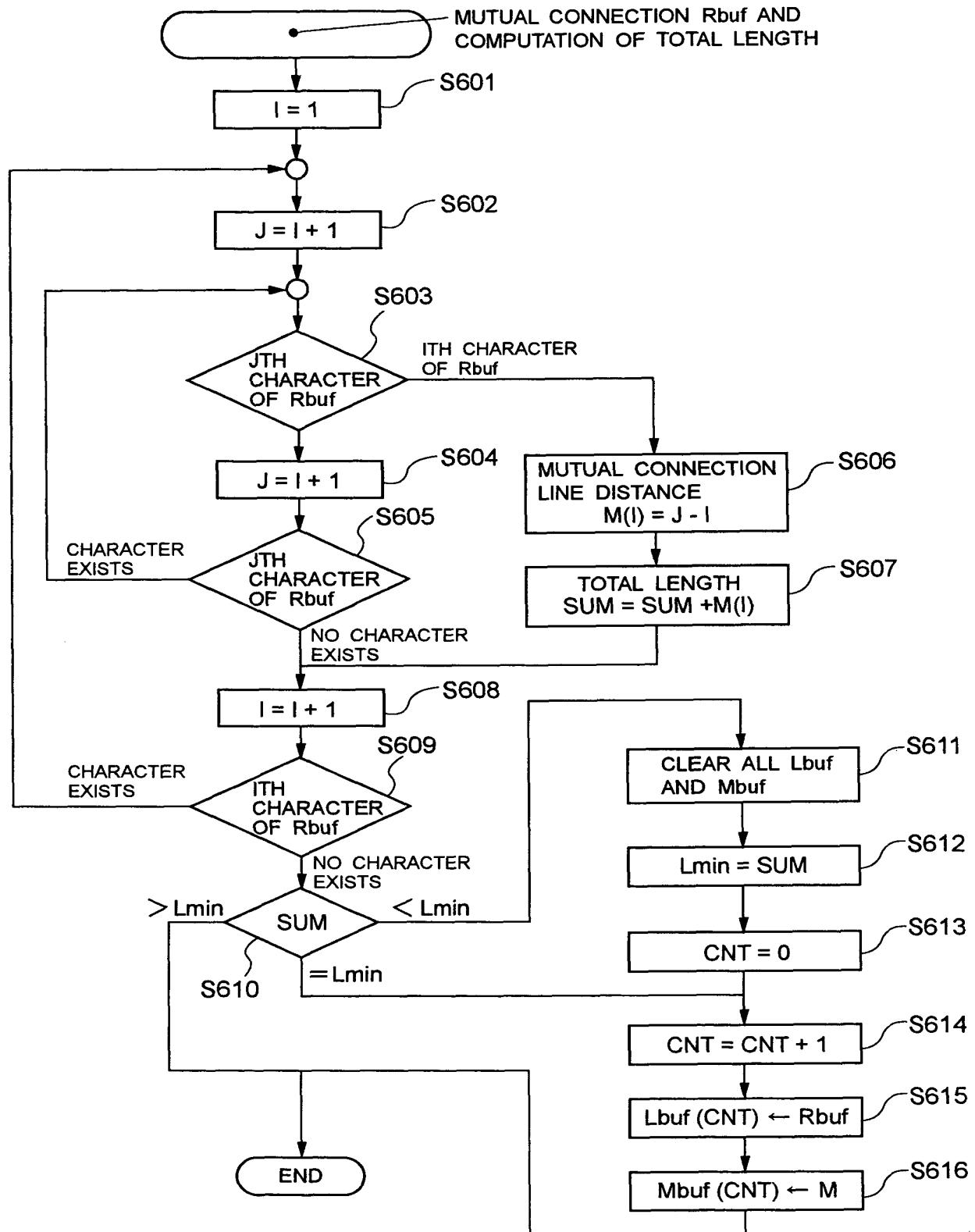
FIG. 26

Cbuf (1)	Cbuf (2)
a F g H h	d G f E e D c B a A b C d l i K e L j J k

Rbuf
a F g H h / d G f E e D c B a A b C d l i K e L j J k
a F g H h / k J j L e K i l d C b A a B c D e E f G d
h H g F a / d G f E e D c B a A b C d l i K e L j J k
h H g F a / k J j L e K i l d C b A a B c D e E f G d
d G f E e D c B a A b C d l i K e L j J k / a F g H h
d G f E e D c B a A b C d l i K e L j J k / h H g F a
k J j L e K i l d C b A a B c D e E f G d / a F g H h
k J j L e K i l d C b A a B c D e E f G d / h H g F a

EXAMPLE OF CONCATENATED ROUTES (Nmin = 2)

FIG. 27



FLOWCHART OF MUTUAL CONNECTION OF Rbuf AND COMPUTATION OF TOTAL LENGTH

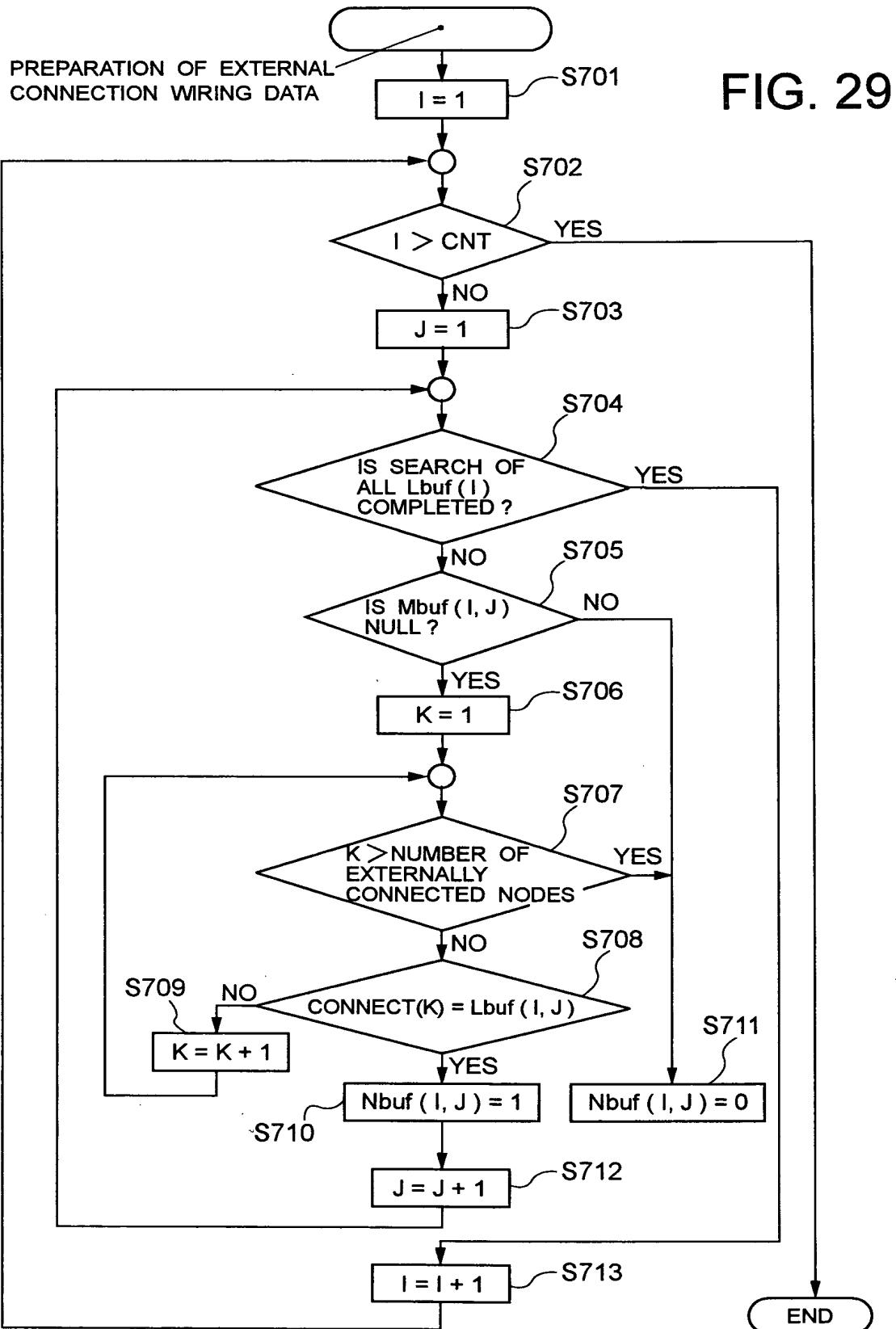
FIG. 28

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	SUM
Rbuf	a	F	g	H	h	/	d	G	f	E	e	D	c	B	a	b	c	d	—	i	K	e	L	j	J	K		
M()	14					12																					38	
Rbuf	a	F	g	H	h	/	k	J	j	L	e	K	i	—	d	C	b	A	a	B	c	D	e	E	f	G	d	
M()	18																										42	
Rbuf	h	H	g	F	a	/	d	G	f	E	e	D	c	B	a	b	c	d	—	i	K	e	L	j	J	K		
M()		10		12			12																				34	
Rbuf	h	H	g	F	a	/	k	J	j	L	e	K	i	—	d	C	b	A	a	B	c	D	e	E	f	G	d	
M()	14																										38	
Rbuf	d	G	f	E	e	D	c	B	a	A	b	C	d	—	i	K	e	L	j	J	k	/	a	F	g	H	h	
M()	12			12			14																				38	
Rbuf	d	G	f	E	e	D	c	B	a	A	b	C	d	—	i	K	e	L	j	J	k	/	h	H	g	F	a	
M()	12																										42	
Rbuf	k	J	j	L	e	K	i	—	d	C	b	A	a	B	c	D	e	E	f	G	d	/	a	F	g	H	h	
M()		12																									34	
Rbuf	k	J	j	L	e	K	i	—	d	C	b	A	a	B	c	D	e	E	f	G	d	/	h	H	g	F	a	
M()		12																									38	

Rbuf AND ARRAY M HAVING SMALLEST SUM
ARE STORED IN Lbuf AND Mbuf

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	Lmin
Lbuf(1)	h	H	g	F	a	/	d	G	f	E	e	D	c	B	a	b	C	d	—	i	K	e	L	j	J	K		
Mbuf(1)		10		12																							34	
Lbuf(2)	k	J	j	L	e	K	i	—	d	C	b	A	a	B	c	D	e	E	f	G	d	/	a	F	g	H	h	
Mbuf(2)		12																									34	

EXAMPLE OF CONCATENATED ROUTES Rbuf, MUTUAL CONNECTION
DATA M AND TOTAL MUTUAL CONNECTION WRING LENGTH



FLOWCHART OF PREPARATION OF EXTERNAL CONNECTION LINE DATA

FIG. 30

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	Nmin	Lmin
Lbuf (1)	h	H	g	F	a	A	b	C	d	/	a	B	C	D	e	E	f	G	d	l	i	K	e	L	j	k	2		
Mbuf (1)												10						8										24	
Nbuf (1)	1	0	1	0	0	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1			
Lbuf (2)	k	J	j	L	e	K	i	l	d	G	f	E	e	D	c	B	a	/	d	C	b	A	a	F	g	H	h	2	
Mbuf (2)																		12										24	
Nbuf (2)	1	0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	0	1			

RESULTS OF EXECUTION OF AUTOMATIC LAYOUT ALGORITHM

FIG. 31

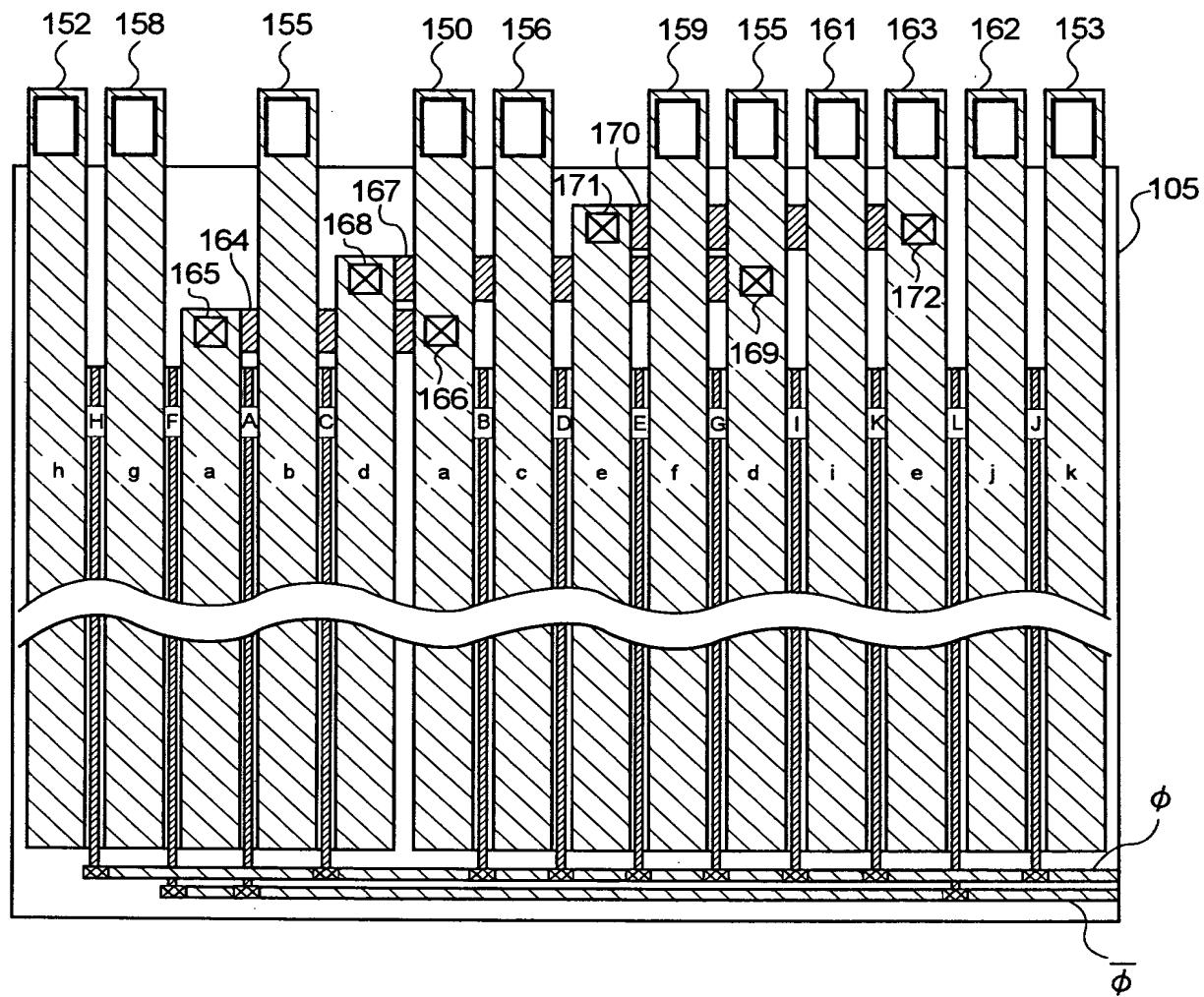
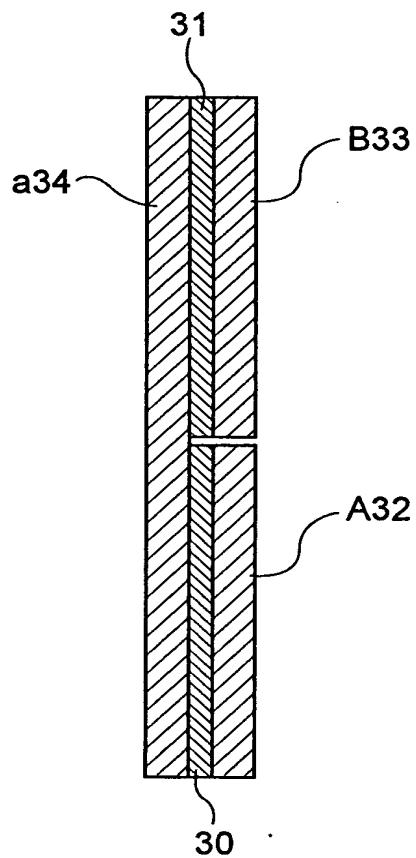
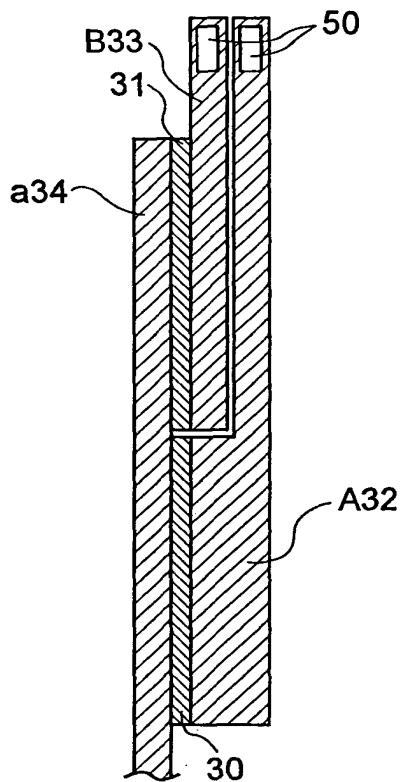


FIG. 32 PRIOR ART



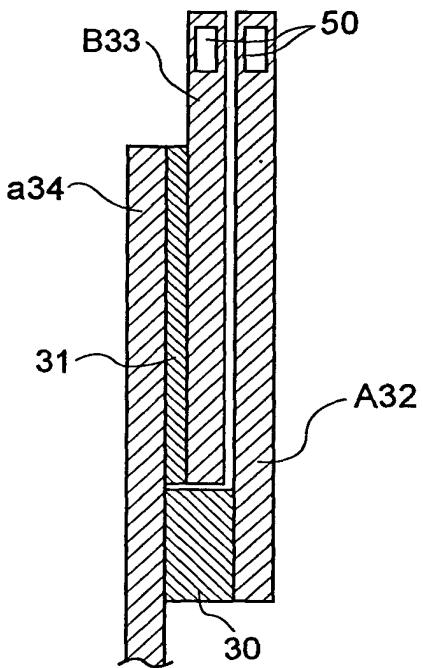
EXAMPLE OF ORDINARY LAYOUT

FIG. 33
PRIOR ART



EXAMPLE OF ORDINARY LAYOUT

FIG. 34
PRIOR ART



EXAMPLE OF ORDINARY LAYOUT